



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,115	04/08/2004	Michael C. Stolowitz	44541/6:2	2463
3528	7590	03/26/2007		
STOEL RIVES LLP 900 SW FIFTH AVENUE SUITE 2600 PORTLAND, OR 97204-1268			EXAMINER WALTER, CRAIG E	
			ART UNIT 2188	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE 3 MONTHS			MAIL DATE 03/26/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,115	STOLOWITZ, MICHAEL C.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Status of Claims

1. Claims 1-31 are pending in the Application.
Claims 1-13, 17, 19-23 and 26-31 are amended.
Claims 1-31 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 14 January 2007 in response to the office action mailed on 13 July 2006 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments. Additionally, Applicant's arguments with respect to claim 17 have been considered but are moot in view of the new ground(s) of rejection. Lastly, several 35 USC § 112 rejections set forth in the previous correspondence (mailed 13 July 2006) were not addressed either by amendment or by Applicant's remarks. These rejections are maintained and restated below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Art Unit: 2188

3. Claim 31 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As for claim 31, the limitation "asserting a common write strobe coupled to all of the FIFO memories" as recited in lines 2-3 is not sufficiently enabled, as one of ordinary skill in the art would not understand how an asserted signal (i.e. strobe) itself can be "coupled to [a memory]". More specifically, one skilled in the art would recognize that only a physical medium itself, carrying said signal could be coupled to the memory (i.e. a bus connection).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 12 and 17-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 12, the phrase "on the fly" renders the claim indefinite, as one of ordinary skill in the art would be unable to ascertain the metes and bounds of this claim limitation. It is assumed that Applicant intended to require "on the fly" to mean dynamic. Similar rejections apply to claim 17.

Claims 18-25 are rejected for further inheriting the deficiencies of claim 17.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-5, 8, 10-12, 14, 16, 26-28, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Searby (US Patent 5,765,186).

As for claims 1 and 10, Searby teaches a method of reading stored data from an array of independent disk drives so as to provide synchronous data transfer into a buffer, the method comprising:

for each disk drive in the redundant array (Fig. 2 elements 21-24),
providing a corresponding FIFO/two-port memory (col. 8, lines 2-6 – RAM buffers (Fig. 2, elements 37-40 are dual port in nature)) for receiving and storing read data responsive to timing signals provided by the respective drive (col. 3, lines 52-67). Also note since data is written in and out sequentially (i.e. the buffers are used to “buffer” data streamed sequentially – i.e. video data - col. 1, lines 7-29), hence the buffer RAMs act as FIFOs;

initiating a READ command to each of the drives of the array, thereby causing each of the drives to retrieve selected elements of its stored data, and to transfer the retrieved data from the drive into its corresponding FIFO/two-port memory using the timing signals provided by the respective drive (col. 5, lines

Art Unit: 2188

38-49 – the control bus is used to in conjunction with request signals (REQ) to indicated a READ command – i.e. when data is to be read from the drives to the RAM buffers);

monitoring each of the FIFO/two-port memories to detect a non-empty condition (col. 7, lines 32-46 – the system transfers the data to the data highway (Fig. 2, element 49) based on the determination that data is stored in the RAM buffers. Since all the buffers receive data substantially concurrently (i.e. all disk stores send data to the RAM buffers at the same time, which causes either all the buffers to contain data, or no buffers to contain data), each RAM is monitored to determine that data is either present (i.e. non-empty condition), or not present. Data present in the RAM buffers is an implied acknowledgment that data have been received from the disk stores. Note the system cannot transfer data to the highway until data is present in the RAM buffers; therefore the memories are monitored for this determination to occur); and

waiting until all of the FIFO/two-port memories indicate such a non-empty condition; then synchronously reading the transferred data from all of the FIFO/two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer (col. 7, lines 32-35 – once all RAMs indicate a non-empty condition (i.e. data is present in each RAM), the data is sent to the data highway and subsequently to the register (i.e. buffer) as shown in Fig. 2, element 50 (see also col. 5, lines 22-37 and col. 6, lines 14-31)). Again, the RAM buffers store data such that either all contain data, or no buffers contain

Art Unit: 2188

data, therefore the data cannot be transferred until all RAM buffers have data (i.e. are non-empty); and

repeating said monitoring, waiting; reading and writing into the buffer steps until completion of a read operation initiated by the said READ command (col. 7, line 62 through col. 8, line 11 – the system will continue the process provided while the request inputted into the controller is present, the concurrent data transfer will not conclude until the request no longer exists (i.e. completion of the READ command)).

As for claim 26, Searby teaches a method of writing data into an array of independent disk drives, the method comprising:

providing a buffer for storing write data (Fig. 2, element 50);

for each disk drive in the array, providing a corresponding two-port memory for receiving and storing write data (Fig. 2, elements 37-40 – the RAM buffers are dual-port as described in the rejection of claim 1);

monitoring each of the two-port memories to detect a non-full condition (col. 7, lines 32-46 – the system transfers the data to the data highway (Fig. 2, element 49) based on the determination that data is stored in the RAM buffers. Since all the buffers receive data substantially concurrently (i.e. all disk stores send data to the RAM buffers at the same time, which causes either all the buffers to contain data, or no buffers to contain data), each RAM is monitored to determine that data is either present (i.e. non-empty condition), or not present. Note the system cannot transfer data to the highway until data is present in the

Art Unit: 2188

RAM buffers; therefore the memories are monitored for this determination to occur);

waiting until all of the two-port memories indicate such a non-full condition; then reading write data from the buffer (again the data is read out of the buffer only when data is present in the buffers. The system must detect that data has been written to the RAM buffers before it can transfer data from each of the RAM buffers to the buffer);

computing redundant data from said write data (col. 9, lines 24-59 – redundant data is calculated base on the information in the buffer);

synchronously storing the write data and the computed redundant data into the two-port memories via a first port of each two-port memory (the parity data and the data to be written are stored concurrently, and are stored via the first port of the dual-port memory – col. 9, lines 24-59); and

while synchronously storing the write data and the computed redundant data into the two-port memories, transferring stored data from a second port of each of the two-port memories into its corresponding disk drive, in each case transferring the previously-stored data responsive to timing control provided by the corresponding disk drive (the controller is responsible for asserting the control signal to enable access for writing to and from each buffer RAM simultaneously. Col. 5, lines 50-62, the data can be either written to or from the RAM buffers and disk stores. The memory is dual-port which permits the system to uniquely assign the functions each of the two ports).

As for claim 3, Searby teaches the method of reading stored data from an array according to claim 1 wherein each two-port memory comprises a FIFO memory (data is written in and out sequentially (i.e. the buffers are used to "buffer" data streamed sequentially – i.e. video data - col. 1, lines 7-29), hence the buffer RAMs act as FIFOs).

As for claim 4, Searby teaches the method of reading stored data from an array according to claim 3 wherein the array comprises a redundant array (col. 3, lines 29-37).

As for claim 5, Searby the method of reading stored data from an array according to claim 4 and further comprising, in the event that one of the disk drives of the redundant array has failed, dynamically regenerating missing data corresponding to the failed drive from the synchronous read data (col. 9, lines 1-39 – parity data is generated and used to replace data in case of a failure).

As for claim 8, Searby teaches the method of reading data from an array according to claim 1 wherein said synchronously reading the stored data from all of the two-port memories comprises asserting a common read enable signal to each of the memories (referring to Fig. 2, the controller (51) asserts the common command line (54) for all RAM buffers to read data from the disk stores).

As for claim 11, Searby teaches the method of reading stored data according to claim 10 wherein the stored data is word striped over the redundant array (col. 4, lines 11-20 and col. 6, lines 14-34 discuss how frames are stored sequentially and striped across each drive. Additionally note the frames are grouped as data words, hence the frames are word striped across the array of disks).

As for claim 12, Searby teaches a method of reading stored data according to claim 10 and further comprising, in the event that one of the disk drives fails to transfer read data to its associated FIFO memory, regenerating the missing read data "on the fly" from the synchronous read data (col. 9, lines 24-60 – the when a error is detected, generated parity information is used account for the error. More specifically, the data regenerator (i.e. data circuitry) performs the bit-wise XOR operation to regenerate missing data due to the drive failure).

As for claim 14, Searby teaches the method of reading data according to claim 10 wherein the synchronous transfer of read data into the common buffer is implemented with a single address counter and a common FIFO read enable signal (referring to Fig. 2, the controller (51) asserts the common command line (54) for all RAM buffers to read data from the disk stores – Additionally, Searby teaches the controller itself as being responsible for generating and counting the addressing to each of the RAM buffers – see Fig. 2).

As for claim 16, Searby teaches a method of reading data from an array according to claim 10 and further comprising providing a FIFO memory in the data path between the individual drive FIFO memories and the common buffer (Fig. 2, elements 4144 depict FIFO buffers between the buffer RAM and the common buffer (50)).

As for claim 27, Searby teaches a method of writing data into an array according to claim 26 and further comprising stalling said storing step whenever any of the two-port memories become full, but only with regard to the full memory, while allowing said synchronously storing the write data to continue into the non-full two-port memories

Art Unit: 2188

(data storage will continue without delay provided the system recognizes that enough free memory is available in the buffer RAM devices – col. 8, lines 1-11).

As for claim 28, Searby teaches a method of writing data into an array according to claim 27 wherein each two-port memory comprises a FIFO memory (data is written in and out sequentially (i.e. the buffers are used to “buffer” data streamed sequentially – i.e. video data - col. 1, lines 7-29), the buffer RAMs act as FIFOs).

As for claim 31, Searby teaches a method of storing data into an array according to claim 28 wherein said synchronously storing the write data into the FIFOs comprises asserting a common write strobe coupled to all of the FIFO memories (referring to Fig. 2, the controller (51) asserts the common command line (54) for all RAM buffers to read data from the disk stores).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Searby (US Patent 5,765,186) as applied to claim 10 above.

As for claim 15, though Searby does not explicitly teach a method of reading data from an array according to claim 10 wherein each synchronous transfer of read data into the common buffer stores 64-bits of read data, such a limitation is merely a matter

of design choice and would have been obvious in the system of Searby. More specifically, Searby teaches his register (Fig. 2, element 50) as storing information 8-bit format rather than 64-bit as claimed by Applicant. The fact that Searby differs by the claimed invention only by the width of the data stored fails to define a patentably distinct invention over Searby, since both the claimed invention and Searby's teachings are both directed synchronous data transfer from asynchronous devices.

7. Claims 6, 7, 13, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Searby (US Patent 5,765,186) as applied to claims 1, 10, and 26 above and in further view of Anderson (US PG Publication 2003/0200478 A1)

As for claims 6, 7, 13, 29, and 30, though Searby teaches all the limitations of claims 1, 10, and 26, he fails to teach the read operation as being effected via corresponding UDMA interface to each of the disk drives (or coupled to each of the drives via the UDMA interface as recited in claim 13).

Anderson however teaches a media server with single chip storage controller, which includes a plurality of storage devices (Fig. 2, element 10, interfaced with a controller (12) over a plurality of communication lines (14). Note Anderson specifically teaches the communication lines as being UDMA interfaces (paragraph 0101, all lines)).

It would have been obvious for Searby to further include Anderson's single chip storage controller into his own system for synchronous data transfer. By doing so, Searby would benefit by having a more efficient RAID storage controller which is integrated to enable rapid recovery from failures as taught by Anderson in paragraph 0006, all lines. Anderson specifically advises the application of this benefit to systems

such as Searby's, which processes video data. Searby would additionally benefit from Anderson's reduction of unwanted interruption by enabling hot swapping of failed drives as taught by Anderson in paragraphs 0016 and 0017, all lines.

8. Claims 2, 9, 17 and 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Searby (US Patent 5,765,186) as applied to claims 1, 17, and 26 above and in further view of Stolowitz (US Patent 6,018,778).

As for claim 17, Searby teaches an improved RAID disk array controller comprising:

- a plurality of disk drive interfaces for attaching physical disk drives (Fig. 2 elements 33-36);

- a two-port memory associated with each of the disk drive interfaces (Fig. 2, elements 37-40 – as discussed with claims 1 and 10, the RAM buffers are FIFO in nature and can be dual-port), each two-port memory arranged to store read data provided by the associated disk drive in a disk read operation and, conversely, to provide write data that was previously-stored in the memory to the associated disk drive in a disk write operation (col. 3, lines 52-67 – data is transferred from the disk stores to the RAM buffers. Conversely, the RAMs may write data to the disk store (col. 5, lines 50-62 – this operation may be reversed to allow the RAMs to write to the disk stores));

- a logic circuit coupled to all of the two-port memories for detecting when all of the two-port memories have data stored therein for a read operation or available space therein for a write operation (col. 7, lines 32-46 – the system transfers the data to the data highway (Fig. 2, element 49) based on the

determination that data is stored in the RAM buffers. Since all the buffers receive data substantially concurrently (i.e. all disk stores send data to the RAM buffers at the same time, which causes either all the buffers to contain data, or no buffers to contain data), each RAM is monitored to determine that data is either present (i.e. non-empty condition), or not present. Data present in the RAM buffers is an implied acknowledgment that data have been received from the disk stores. Note the system cannot transfer data to the highway until data is present in the RAM buffers; therefore the memories are monitored for this determination to occur (his operation is controlled by the controller (i.e. logic circuit) which is coupled to the RAMs));

control circuitry responsive to the logic circuit for synchronously reading data from all of the two-port memories only when all of the two-port memories have data stored therein, thereby forming synchronous read data (col. 7, lines 32-35 – once all RAMs indicate a non-empty condition (i.e. data is present in each RAM), the data is sent to the data highway and subsequently to the register (i.e. buffer) as shown in Fig. 2, element 50 (see also col. 5, lines 22-37 and col. 6, lines 14-31)). Again, the RAM buffers store data such that either all contain data, or no buffers contain data, therefore the data cannot be transferred until all RAM buffers have data (i.e. are non-empty). The controller, via the aid of SCSI interface logic; controls this function;

the control circuitry further responsive to the logic circuit for detecting that all of the two-port memories have space therein and synchronously writing data

to all of the two port memories thereby forming synchronous write data (the system will continue to buffer the data if it is determined that space is available to stream more data (col. 7, line 62 through col. 8, line 11));

first redundant data circuitry for regenerating missing data "on the fly" from the synchronous read data in the event that one of the disk drives fails to provide read data to its associated two-port memory in a read operation (col. 9, lines 24-60 – the when a error is detected, generated parity information is used account for the error. More specifically, the data regenerator (i.e. data circuitry) performs the bit-wise XOR operation to regenerate missing data due to the drive failure); and

second redundant data circuitry for generating redundant data "on the fly" from the synchronous write data for storing in the array (col. 9, lines 1-39 – the last drive of the array is used to store parity information. In case of a drive failure, the data in this last disk store can be used to generate the data needed to correct the drive failure) and wherein:

Searby however fails to teach one of the disk interfaces as being specifically connected to a redundant disk wherein the first redundant circuitry regenerates corrected in the event of a failed drive without delaying the output of the read data as recited by Applicant in the instant claim.

Stolowitz however teaches a disk array controller including:

Art Unit: 2188

one of the disk drive interfaces is designated for connection to a redundant disk drive for storing redundant data so that the synchronous read data includes redundant data (col. 13, line 55 through col. 14, line 3 – the drives include a redundant drive) ;

the first redundant data circuitry for regenerating missing data is coupled to all of the memories to receive the synchronous read data, including the redundant data, and further is arranged to compute a redundant data operation across the synchronous read data so as to provide corrected data in the event of a failed drive without delaying output of the read data (col. 8, lines 25-65 – once a drive fails, the system can reconstruct the lost data, and continue to perform the necessary step for data transfer by excluding the drive that failed. Note Stolowitz explicitly teaches no delay occurring during this process).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Searby to further include Stolowitz's disk array controller and method to synchronously transfer data into his own system of synchronously transferring data. By doing so, Searby would benefit by improving his own disk array performance and improve his disk array storage reliability while reducing the cost and complexity of his present controller to perform a synchronous data transfer as taught by Stolowitz (col. 6, lines 4-18).

As for claim 19, Searby teaches an improved RAID disk array controller according to claim 17 wherein each two-port memory comprises a FIFO memory data is written in and out sequentially (i.e. the buffers are used to "buffer" data streamed sequentially – i.e. video data - col. 1, lines 7-29, the buffer RAMs act as FIFOs).

As for claim 21, Searby teaches an improved RAID disk array controller according to claim 17 and further comprising a single address counter arranged for addressing the buffer for transfers between the buffer and the FIFO memories in either direction (the controller itself is responsible for generating and counting the addressing to each of the RAM buffers – see Fig. 2 – Additionally note the data transfer can occur either from disk stores to the RAM buffers or vice versa – col. 5, lines 50-62).

As for claim 9, though Searby teaches the method of reading data from an array according to claim 1, he fails to teach wherein said synchronously reading the stored data from all of the two-port memories is conducted over a single DMA channel.

Stolowitz however teaches a disk array controller that synchronously transfers data between data port and a buffer memory, which uses a single DMA channel to interface between the drives and the memories (col. 11, lines 5-24).

As for claim 2, Stolowitz teaches the stored data includes as including user data as well as redundant data sufficient to enable reconstruction of all of the user data in the event of a failure of any single drive of the array and the method further comprising, in the event that one of the disk drives fails, executing said initiating, monitoring, waiting and synchronously reading steps only with respect to the non-failed drives; and dynamically regenerating missing data corresponding to the failed drive from the synchronous read data (col. 8, lines 25-65 – once a drive fails, the system can reconstruct the lost data, and continue to perform the necessary step for data transfer by excluding the drive that failed).

As for claim 20, Stolowitz teaches a buffer comprising DRAM (Fig. 6, element 106).

As for claims 22-23, Stolowitz teaches all drives implement a ATA/ATAPI interface (Fig. 2, all drives are IDE – Stolowitz discusses the equivalence of IDE and ATA – col. 4, lines 1-10). Note this similar comparison is discussed in Applicant's original specification paragraph 0005.

As for claim 24, Stolowitz teaches the array controller as being implemented on a signal motherboard (col. 13, line 57 through col. 14, line 3).

As for claim 25, Stolowitz teaches the array controller as being implemented on a Host Bus Adapter (Fig. 2, element 104 - since a host bus adapter is defined as "a device for connecting a peripheral to the main computer", the host interface serves as a host bus adapter as it interfaces the array controller and disks with the host itself via the host bus (Fig. 2, element 102)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Searby to further include Stolowitz's disk array controller and method to synchronously transfer data into his own system of synchronously transferring data. By doing so, Searby would benefit by improving his own disk array performance and improve his disk array storage reliability while reducing the cost and complexity of his present controller to perform a synchronous data transfer as taught by Stolowitz (col. 6, lines 4-18).

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Searby (US Patent 5,765,186) and Stolowitz (US Patent

Art Unit: 2188

6,018,778) as applied to claim 17 above, and in further view of Yamamoto (US Patent 5,801,859).

As for claim 18, though the combined teachings of Searby and Stolowitz disclose, allowing the dual port memory to transfer data in either direction via unique I/O ports, they fail to teach exchanging them via multiplexers as claimed by Applicant. Yamamoto however teaches a network system for plural node devices without arbitration, in which the port (either input or output) can be exchanged via multiplexing logic (col. 30, lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Searby and Stolowitz to further include Yamamoto's system into his own system for synchronously transferring data. By doing so, they would benefit by having a more efficient means of data transfer while preventing the need for increased hardware costs as taught by Yamamoto in col. 5, lines 51-67.

Response to Arguments

10. Applicant's amendments and arguments with respect to the 35 USC 102(e) rejections set forth against claims 1 and 10, and the 35 USC 103(a) rejections set forth have been fully considered, but they are not persuasive. Additionally, Applicant's arguments with respect to claim 17 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2188

As for claim 1, Applicant contends, "Searby synchronizes data transfer from the drives to the RAM buffer; Applicant's method of claim 1 leaves those transfers asynchronous." Applicant additionally alleges, " Searby (FIG. 2) waits until all of the disc interfaces (SCSI 33-36) have data ready, as indicated by the REQ commands:", whereas "Applicant's method of claim 1 - does NOT wait for each drive interface to signal "data ready." To the contrary, the data is transferred, per Applicant's claim 1, "from the drive into its corresponding two-port memory using the timing signals provided by the respective drive."

This argument however is not persuasive. First, Examiner contends that Applicant does in fact describe synchronizing the data transfer from drives to the buffer notwithstanding Applicant's contention otherwise. More specifically, the preamble of Applicant's instant claim 1 recites, "[a] method of reading stored data from an array of independent disk drives so as to provide **synchronous data transfer** into a buffer..." (emphasis added). The claim additionally recites "synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer". Applicant's argument is not persuasive since Applicant concedes by his own admission that Searby synchronizes data transfer from the drives to the RAM buffer, as similarly recited by Applicant in the preamble.

Additionally, Examiner maintains that Searby does in fact teach the limitation "transfer[ring] the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive" counter to Applicant's

assertion. Referring again to Searby in Fig. 2, and col. 5, lines 39-49, a request signal is associated with each respective drive, in order to control the transfer of information. Applicant's attempt to assert that Searby's system operates in some alternative manner as recited in the instant claim (i.e. Applicant's summary of Searby's Fig. 1) is not persuasive, as Examiner maintains (as stated in the original rejection) that Fig. 2, not Fig. 1, along with col. 5, lines 39-49 of Searby in fact teach this limitation per the arguments and rejection discussed *supra*.

Applicant additionally asserts, "[t]he claim step of 'monitoring each of the two-port memories to detect a non-empty condition' is not taught in Searby. Searby actually 'monitors' the RAM buffer (likely counts write commands or checks current RAM addresses) in order to transfer data to the highway 49 upon completion of a frame of video data." Applicant further contends, "[the] Searby [process] is all synchronous and for that reason the controller really has no need at all to 'monitor each of the two-port memories to detect a non-empty condition.'" That need arises in Applicant's method of claim 1 precisely because the two-port memories are receiving data asynchronously (each memory using the timing signals provided by the respective drive, as discussed above)." Lastly Applicant asserts, "the data in Searby was already synchronized as it was written into the RAM buffer as discussed earlier".

This argument however is not persuasive. Examiner maintains that memory monitoring to some degree is inherent in a system such as Searby's. More specifically, before Searby's system is capable of transferring data to the data highway and ultimately to the buffer (col. 7, lines 32-35), the system must in fact determine that data

Art Unit: 2188

is stored in each of the buffers (since Searby's system is directed to the parallel transfer of data, the system must wait until each of the memories has data present before the data can be sent to the highway). Since Searby must wait until data is present before it can be stored, his system must inherently perform some sort of monitoring process of the memories to determine if data is present to transfer (i.e. non-empty condition), hence it is inherent. Since Examiner has no intrinsic evidence from Applicant's specification to rely upon to further define "monitoring" (i.e. a definition of "monitoring" is not explicitly addressed within the specification), Examiner is forced to rely upon extrinsic evidence for which to interpret the term "monitoring". One of ordinary skill in the art would understand "monitoring" to include "the observation, detection, or recording of an operation of a machine or system" (standard English dictionary definition), therefore Examiner has properly applied this definition against the claims as being the "broadest reasonable interpretation consistent with Application specification" pursuant to MPEP § 2111. Since Searby's system must inherently observe or detect if data is stored in each memory before said data can be transferred (otherwise the system would be incapable of accessing the data stored therein), Searby in fact anticipates this limitation. Assuming *arguendo* that Applicant's characterization of Searby is correct, in that Searby's data is already synchronized as it was written into the RAM buffer (therefore it is not *forming* synchronous read data); Applicant's arguments would still not be persuasive. More specifically, synchronous data is formed and written at least by the time it is transmitted, hence Searby does in fact teaches "synchronously

reading the transferred data from all of the two-port memories”, therefore the data *formed* from this transmission is in fact synchronous as required by the instant claim.

Applicant’s arguments with respect to claim 17 are rendered moot in view of the new ground of rejection necessitated by Applicant’s amendment.

Applicant’s arguments with respect to all claims previously rejected under 35 USC 103(a) (i.e. sections B through E of Applicant’s remarks – page 17) as being allowable for depending upon a allegedly allowable base claim is rendered moot, and Examiner maintains that all base claims remain either anticipated or rendered obvious per the rejections and arguments set forth *supra*.

Conclusion

11. Applicant’s amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

12. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

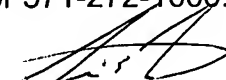
Art Unit: 2188

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Craig E Walter
Examiner
Art Unit 2188

CEW


HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

3-21-07